UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,194	09/28/2001	Victor Key Pecone	4430-32	6054

22442 7590 06/22/2007

SHERIDAN ROSS PC
1560 BROADWAY
SUITE 1200
DENVER, CO 80202

EXAMINER	
PEYTON, TAMMARA R	
ART UNIT	**PAPER NUMBER**
2182	

MAIL DATE	DELIVERY MODE
06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/967,194	PECONE, VICTOR KEY	
	Examiner	Art Unit	
	Tammara R. Peyton	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :9/23/04, 5/9/05, 5/16/05, 6/8/05, 1/10/07, 1/22/07.

DETAILED ACTION

Response to Restriction Argument

Applicant argues that Species 1-3 are not patentably distinct and are not a burden. Examiner disagrees with Applicant. Species II has separate utility such as "a method for transferring data between a host computer and one or more storage devices, comprising: transferring firstly data from the host computer to a channel interface module using a first channel medium; transferring secondly said data from said channel interface module to a first controller memory module using a passive backplane; processing said data at said controller memory module to define storage data; transferring thirdly said storage data to said channel interface module via said passive backplane; transferring fourthly said storage data to the at least one storage device via a second channel medium; and mirroring said storage data between said first controller memory module and a second controller memory module substantially independently of said first Channel medium and said second channel medium," and Species III, has a separate utility such as "a network storage apparatus for connecting a host computer with at least one storage device, comprising: at least first and second channel interface modules, each adapted to be connected to a host channel and a disk channel, that are operational to send and receive data over the host channel and disk channel, the host channel being connected to the host computer and the disk channel being connected to the at least one storage device; at least first and second controller memory modules that communicate with said first and second channel interface modules and process

data from the host computer to provide storage data for storage on the at least one storage device and process data from the at least one storage device to provide retrieved data for delivery to the host computer; and a passive backplane connected to each of said channel interface modules and each of said controller memory modules that supports communication between said channel interface modules and said controller memory modules, wherein when data is being carried by the host channel and/or the disk channel and at the same time data isbeing mirrored between said first controller memory module and said second controller memory module, neither the host channel nor the disk channel carries more than fifty per cent of said data being mirrored." Inventions 1-3 are patentably distinct. Applicant's arguments are not persuasive and the restriction rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al., (sited as prior art 05/09/05) and Walton et al., (US 6,687,797).

As per claims 1, 2, 3, 5, and 7-9, Kitamura teaches a network storage apparatus (4) for connecting a host computer (1a...1n) with at least one storage device (21, Fig.

1, 2a-2m, Figs. 8, 18), comprising: a plurality of data buses (Figs. 8, 18) including first and second data buses; at least first and second channel interface modules (Fig.18, between the interface 12 and the port 81) connected to and adapted to be connected to the host computer and the at least one storage device, that are operational to send and receive storage data to and from the host computer and the at least one storage device and that are operational to selectively transfer the storage data to one or more of said plurality of data buses; and at least first and second controller memory modules (channel processors, Figs. 8, 18),, connected to said passive backplane, that communicate with said channel interface modules and that store and process the storage data transferred to and from said channel interface modules. Kitamura teaches a network storage system that is adapted to be connected to a host computer and at least one storage device (21, Fig.1 or 2a-2m, Fig. 8), wherein storage data is sent between a host and a storage device via interface 12 and fibre channel switch 8. The interface 12, reading onto the communication path portion, transfers storage data between the host and the communication path portion and between the storage device and the communication path portion as it controls all data transfers on the link between the host and port 81. However, Kitamura is silent in respect to the use of a passive backplane having a plurality of data buses. It would have been obvious to one of ordinary skill at the time the invention was made that the use of a passive backplane is well known in the art. Nonetheless, Walson teaches the use of a passive backplane in that it has no active electronic circuitry mounted on or in it; it is just a passive communications medium. Walson discloses that the passive backplane can be

essentially comprised of just one or more substantially planar substrate layers (which may be conductive or which may be dielectric with conductive traces disposed on/in it), with various pin-and-socket type connectors mounted on it to allow connection to other components. (Walson, col. 9, lines 38-col. 12, lines 1-28) Therefore, it would have been be obvious to a person skilled in the art in the system disclosed in Kitamura that currently uses a fibre channel switch 8, implement a passive backplane with a plurality of buses, as disclosed by Walson because doing so would add and expand the flexibility of Kitamura's system without departing from the inventive concept.

As per claim 3, Kitamura-Walson teaches wherein at least one backplane interface that connects to said passive backplane; a memory interface that connects to said memory; a processing interface that connects to said processing portion; a bridge core that contains control logic operable to connect said processing interface, memory interface and backplane interface; and at least one of an exclusive OR (XOR) engine that performs XOR functions on data blocks. Specifically, Walson teaches a direct memory access (DMA) engine (Fig. 7) that provides DMA access to said passive backplane.

As per claim 6, Kitamura-Walson discloses wherein each of said first and second data buses is part of a group of backplane buses, however Kitamura-Walson do not expressly teach wherein said group includes peripheral component interconnect (PCIX) buses. However, PCIX buses are well known in the art thereby making use of this type

of bus obvious to one skilled in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (571) 272-4157. The examiner can normally be reached between 6:30 - 4:00 from Monday to Thursday, (I am off every first Friday), and 6:30-3:00 every second Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3718. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(703) 872-9306

Hand-delivered responses should be brought to:

USTPO, 2011 South Clark Place, Customer Window

Crystal Plaza Two, Lobby Room 1B03, Arlington, VA, 22202Crystal Park II, 2121.

TAMMARA PEYTON
PRIMARY EXAMINER

Tammara Peyton

June 16, 2007